IN THE CLAIMS:

1. (Currently Amended) A signal processing device comprising a plurality of functional units (UC1-UCn) for processing digital data based on an instruction word, ~~and~~

a plurality of register files (RF1-RFn) for storing results obtained from respective ones of said functional units, wherein said functional units are arranged to write a result to a predetermined register of said register files by using a register address (RRI) derived from said instruction word, and,

~~characterized by~~

register allocation means (RA) for selecting at least two of said register files (RF1-RFn) and for supplying said register address to said selected register files, if said instruction word comprises a corresponding indication.

2. (Currently Amended) [[A]] The device according to claim 1, ~~characterized in that~~ wherein said functional units (UC1-UCn) are arranged to supply said corresponding indication to said register allocation means (RA).

3. (Currently Amended) [[A]] The device according to claim 1, ~~characterized in that~~ wherein said signal processing device is a programmable VLIW processor, and said register files are partitioned register files (RF1-RFn), wherein a data stationary instruction encoding is used.

4. (Currently Amended) [[A]] The device according to claim 1, ~~characterized in that~~ wherein said corresponding indication is an information stating that said result is to be written to said register address of said selected register files.

5. (Currently Amended) [[A]] The device according to claim 1, ~~characterized in that~~ wherein said corresponding indication is a result index (RI) which refers to a multicast or broadcast register in said selected register files.

6. (Currently Amended) [[A]] The device according to claim 1, ~~characterized in that~~ wherein said register allocation means comprises demultiplexing means (DM1-DM3) for demultiplexing said result and said register address (RRI) to said selected register files in response to said corresponding indication.

7. (Currently Amended) [[A]] The device according to claim 1, ~~characterized in that~~ wherein said functional units are functional unit clusters (UC1-UCn).

8. (Currently Amended) A method of supplying a signal processing result to a plurality of registers arranged in different register files (RA1-RAn) of a signal processing device, said method comprising the steps of:

a) determining a register address (RRI) based on an instruction word, ~~and~~

b) supplying said register address to said plurality of register files,

~~characterized by the steps of~~ and,

c) selecting said ~~different~~ plurality of register files based on a corresponding indication in said instruction word and supplying said register address to said selected register files.

9. (Currently Amended) [[A]] The method according to claim 8, ~~characterized in that~~ wherein said corresponding indication is an information stating that said result is to be written to said register address of said selected register files.

10. (Currently Amended) [[A]] The method according to claim 8,

~~characterized in that~~ wherein

said corresponding indication is a result index (RI) which refers to a multicast or broadcast register in said selected register files.

11. (Currently Amended) [[A]] The method according to claim 8, ~~characterized in that~~ wherein said selection step comprises a demultiplexing step of demultiplexing said result and said register address to said selected register files in response to said corresponding indication.